In the Claims:

Please add the following new claims:

81.(New) A memory device comprising:

internal circuitry configured to program reference cells within the memory device, wherein said internal circuitry utilizes existing array cell to reference cell comparison circuitry for determining a program level of at least one of said reference cells.

82.(New) A method of programming a reference cell in a device, comprising the step of:

programming a threshold voltage of said reference cell utilizing internal circuitry of the device, wherein said step of programming a threshold level includes the step of applying array cell programming circuitry to said at least one reference cell to program said at least one reference cell.

83. A method of programming a reference cell in a device, comprising the step of:

programming a threshold voltage of said reference cell utilizing internal circuitry of the device, wherein said step of programming a threshold level includes the step of:

applying array cell to reference cell comparison circuitry to determine a program level of said at least one reference cell.

84.(New) A method of programming a reference cell in a device, comprising the step of:

programming a threshold voltage of said reference cell utilizing internal circuitry of the device, wherein said step of programming a threshold level includes the steps of:

programming said reference cells utilizing control circuitry of said internal circuitry; and

evaluating a programmed state of at least one of said reference cells by comparing the programmed state against a predetermined reference level.

85.(New) The method according to claim 84, wherein said step of evaluating includes the steps of:

applying array cell evaluation voltages to a selected array cell;

applying reference cell evaluation voltages to a reference cell to be evaluated; and

calculating a programmed state of the reference cell to be evaluated using at least one of said array cell evaluation voltages, said reference cell evaluation voltages, and currents flowing through each of said selected array cell and the reference cell to be evaluated to determine a programmed state of said reference cell.

86.(New) The method according to claim 84, wherein said step of evaluating includes the steps of:

adjusting a gate voltage applied to at least one of the reference cells to be evaluated and said selected array cell until a current flowing in each of said selected array cell and the reference cell to be evaluated are equal; and

calculating a programmed state of the reference cell to be evaluated based on a difference in gate voltages between said selected array cell and the reference cell to be evaluated.

87.(New) The method according to claim 84, wherein said step of evaluating includes the steps of:

adjusting a gate voltage applied to at least one of the reference cells to be evaluated and said selected array cell until a ratio of currents flowing in each of said selected array cell and the reference cell to be evaluated comprises a predetermined ratio; and

calculating a programmed state of the reference cell to be evaluated based on a difference in gate voltages between said selected array cell and the reference cell to be evaluated, and said predetermined ratio.

88.(New) The method according to claim 84, wherein said step of evaluating includes the steps of:

applying a source current to a reference cell to be evaluated; and

adjusting a gate voltage the reference cell to be evaluated until one of a stop and start of a predetermined level of current is sourced by the reference cell to be evaluated indicating a programmed state of the reference cell to be evaluated.

89.(New) The method according to claim 85, wherein:

said step of applying array cell evaluation voltages includes at least one step of,

applying at least one external voltage source to said selected array cell,

dividing at least one of an external voltage and an internal voltage source and applying the divided voltage to said selected array cell, and

retrieving a table register value indicating at least one voltage and applying the indicated voltages to said selected array cell; and

said step of applying reference cell evaluation voltages to a reference cell to be evaluated includes at least one step of,

applying at least one external voltage source to the reference cell to be evaluated,

dividing at least one of an external voltage and an internal voltage source and applying the divided voltage to the reference cell to be evaluated, and

retrieving a table register value indicating at least one voltage and applying the indicated voltages to the reference cell to be evaluated.

90.(New) A method of programming a reference cell in a device comprising the steps of:

programming a threshold voltage of said reference cell utilizing internal circuitry of the device;

verifying the programmed threshold of said reference cell; and

repeating said steps of programming and verifying until one of a max number of programming attempts has occurred and a predetermined threshold voltage is attained in said reference cell.

91.(New) A method of programming a reference cell in a device, comprising the step of:

programming a threshold voltage of said reference cell utilizing internal circuitry of the device, wherein said step of programming a threshold voltage comprises the steps of,

determining if said threshold voltage has at least attained a predetermined program level via a program verify operation;

if said threshold voltage has not attained said predetermined programmed level, then performing the step of,

programming the reference cell; and

repeating said steps of determining and programming until at least one of a max number of program attempts occurs and said predetermined program level is attained in said reference cell.

92.(New) The method according to claim 91, further comprising the step of:

verifying the programmed threshold of said reference cell.

93.(New) A memory device, comprising:

at least one array cell configured to store data;

at least one reference cell configured to provide a reference for operations performed on said array cells;

means for performing said operations on said array cells utilizing said reference cells; and

means for programming said reference cells utilizing internal circuitry of said memory device.

94.(New) The memory device according to claim 93, wherein said memory device is a flash memory device.

95.(New) A memory device comprising:

at least one array cell configured to store data;

at least one reference cell configured to provide a reference for operations performed on said array cells;

means for performing said operations on said array cells utilizing said reference cells; and

means for programming said reference cells utilizing internal circuitry of said memory device, wherein said means for programming includes:

means for determining a threshold voltage (V_T) of a selected reference cell by comparing the selected reference cell to a selected array cell; and

means for programming the selected reference cell to a selected V_T based on the determined threshold voltage (V_T).

96.(New) A memory device comprising:

at least one array cell configured to store data;

at least one reference cell configured to provide a reference for operations performed on said array cells;

means for performing said operations on said array cells utilizing said reference cells; and

means for programming said reference cells utilizing internal circuitry of said memory device, wherein said means for programming comprises:

means for producing high level voltages, internal to said device and controlled by said means for performing, for applying programming pulses to said reference cell arrays.

Appendix

Pending Claims

(Claims 1-62 have been cancelled.)

63. A method of operating a nonvolatile memory comprising the steps of:

programming a plurality of threshold voltages in a reference storage, the threshold voltages defining a plurality of data states of an individual memory cell of the nonvolatile memory;

electrically erasing selected ones of the programmed plurality of threshold voltages in the reference storage; and

fine-tune programming the selected ones of the programmed plurality of threshold voltages in the reference storage.

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64. A method according to claim 63 further comprising the steps of:

sensing a voltage from an individual memory cell of the nonvolatile memory;

sensing a plurality of programmed threshold voltages from the reference storage;

comparing the sensed voltage from the individual memory cell to the sensed plurality of programmed threshold voltages from the reference storage; and

determining a multiple-bit data value based on the comparison result.

65. A method according to claim 63 wherein the step of programming a plurality of threshold voltages in a reference storage further comprises the steps of:

programming an individual electrically-erasable reference cell to define a plurality of data states in the individual memory cell of the nonvolatile memory.

66. A method according to claim 63 wherein the step of programming a plurality of threshold voltages in a reference storage further comprises the steps of:

programming a plurality of electrically-erasable reference cells to define a plurality of data states in the individual memory cell of the nonvolatile memory.

67. A method according to claim 63 wherein the step of programming a plurality of threshold voltages in a reference storage further comprises the steps of:

programming a plurality of electrically-erasable reference cells to define a plurality of data states in the individual memory cell of the nonvolatile memory; and

programming individual electrically-erasable reference cells of the plurality of electrically-erasable reference cells to define a plurality of data states in the individual memory cell of the nonvolatile memory.

68. An electronic system including a processor, a memory and a system bus comprising:

a memory circuit performing the method according to claim 63.

69. A memory circuit for operating a nonvolatile memory comprising:

a reference storage;

means coupled to the reference storage for programming a plurality of threshold voltages in the reference storage, the threshold voltages defining a plurality of data states of an individual memory cell of the nonvolatile memory;

means coupled to the reference storage for electrically erasing selected ones of the programmed plurality of threshold voltages in the reference storage; and

means coupled to the reference storage for fine-tune programming the selected ones of the programmed plurality of threshold voltages in the reference storage.

70. A memory circuit according to claim 69 further comprising:

means for sensing a voltage from an individual memory cell of the nonvolatile memory;

means coupled to the reference storage for sensing a plurality of programmed threshold voltages from the reference storage;

means coupled to the reference storage and coupled to the nonvolatile memory for comparing the sensed voltage from the individual memory cell to the sensed plurality of programmed threshold voltages from the reference storage; and

means coupled to the comparing means for determining a multiple-bit data value based on the comparison result.

71. A memory circuit according to claim 69 wherein the means for programming a plurality of threshold voltages in a reference storage further comprises:

means for programming an individual electrically-erasable reference cell to define a plurality of data states in the individual memory cell of the nonvolatile memory.

72. A memory circuit according to claim 69 wherein the means for programming a plurality of threshold voltages in a reference storage further comprises:

means for programming a plurality of electrically-erasable reference cells to define a plurality of data states in the individual memory cell of the nonvolatile memory.

73. A memory circuit according to claim 69 wherein the means for programming a plurality of threshold voltages in a reference storage further comprises:

means for programming a plurality of electrically-erasable reference cells to define a plurality of data states in the individual memory cell of the nonvolatile memory; and

means for programming individual electrically-erasable reference cells of the plurality of electrically-erasable reference cells to define a plurality of data states in the individual memory cell of the nonvolatile memory.

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74. A memory circuit according to claim 69 wherein the nonvolatile memory is flash electrically-erasable and programmable memory.

75. A circuit comprising:

an interface circuit for interfacing to a nonvolatile memory, the nonvolatile memory including an individual memory cell, the interface circuit including a comparing circuit for comparing a data level of the individual memory cell to a reference data level;

a programmable and electrically erasable reference cell circuit generating the reference data level of a plurality of reference data levels defining a plurality of data states of the individual memory cell;

a first plurality of conductive lines coupling the interface circuit to the reference cell circuit;

a second plurality of conductive lines for coupling the interface circuit to an erase voltage source; and

a plurality of switches alternatively blocking the first plurality of conductive lines while coupling the second plurality of conductive lines and coupling the first plurality of conductive lines while blocking the second plurality of conductive lines.

76. A memory comprising:

an array cell having an output, an array threshold value set to one of n array threshold values to control a signal provided at the array cell output, and a gate;

a reference cell having an output, a floating gate which stores an electrical charge to allow a reference threshold value to be programmed, and a gate, the reference cell having its reference threshold value programmed between two successive ones of the n array threshold values to control a signal provided at the reference cell output;

a comparison circuit coupled to the array cell output and the reference cell output, the comparison circuit for comparing the signal at the array cell output to the signal at the reference cell output and providing a signal indicating which of the n array threshold values is held by the array cell; and

a power supply for supplying a supply voltage to the gate of the array cell to enable the array cell to provide the signal at the array cell output, the power supply further supplying the supply voltage to the gate of the programmable reference cell to enable the reference cell to provide the signal at the reference cell output.

77. The memory of claim 76 wherein when a value of the supply voltage is varied, a working margin between the array cell output and the reference cell output remains constant.

78. The memory of claim 76 wherein n is greater than two.

79. A memory comprising:

a first word line;

a second word line;

a power supply for providing a substantially identical supply voltage to the first word line and the second word line;

an array cell having a gate connected to the first word line and a source-to-drain path, the array cell having a threshold value set to one of n array threshold values;

n-1 read reference cells, each read reference cell having a gate connected to the second word line, a source-to-drain path and a floating gate which stores an electrical charge to allow a reference threshold value to be programmed, each respective read reference cell having its reference threshold value programmed between two different successive ones of the n array threshold values; and

read sense amplifiers, each read sense amplifier having a first input coupled to the source-to-drain path of the array cell and a second input coupled to the source-to-drain path of a respective one of the read reference cells, each read sense amplifier for providing an output signal indicating whether a signal received at its first input is greater than a signal received at its second input.

80. The memory of claim 79 wherein n is greater than two.

81.(New) A memory device comprising:

internal circuitry configured to program reference cells within the memory device, wherein said internal circuitry utilizes existing array cell to reference cell comparison circuitry for determining a program level of at least one of said reference cells.

82.(New) A method of programming a reference cell in a device, comprising the step of:

programming a threshold voltage of said reference cell utilizing internal circuitry of the device, wherein said step of programming a threshold level includes the step of applying array cell programming circuitry to said at least one reference cell to program said at least one reference cell.

83. A method of programming a reference cell in a device, comprising the step of:

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applying array cell to reference cell comparison circuitry to determine a program level of said at least one reference cell.

84.(New) A method of programming a reference cell in a device, comprising the step of:

programming a threshold voltage of said reference cell utilizing internal circuitry of the device, wherein said step of programming a threshold level includes the steps of:

programming said reference cells utilizing control circuitry of said internal circuitry; and

evaluating a programmed state of at least one of said reference cells by comparing the programmed state against a predetermined reference level.

85.(New) The method according to claim 84, wherein said step of evaluating includes the steps of:

applying array cell evaluation voltages to a selected array cell;

applying reference cell evaluation voltages to a reference cell to be evaluated; and

calculating a programmed state of the reference cell to be evaluated using at least one of said array cell evaluation voltages, said reference cell evaluation voltages, and currents flowing through each of said selected array cell and the reference cell to be evaluated to determine a programmed state of said reference cell.

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86.(New) The method according to claim 84, wherein said step of evaluating includes the steps of:

adjusting a gate voltage applied to at least one of the reference cells to be evaluated and said selected array cell until a current flowing in each of said selected array cell and the reference cell to be evaluated are equal; and

calculating a programmed state of the reference cell to be evaluated based on a difference in gate voltages between said selected array cell and the reference cell to be evaluated.

87.(New) The method according to claim 84, wherein said step of evaluating includes the steps of:

adjusting a gate voltage applied to at least one of the reference cells to be evaluated and said selected array cell until a ratio of currents flowing in each of said selected array cell and the reference cell to be evaluated comprises a predetermined ratio; and

calculating a programmed state of the reference cell to be evaluated based on a difference in gate voltages between said selected array cell and the reference cell to be evaluated, and said predetermined ratio.

88.(New) The method according to claim 84, wherein said step of evaluating includes the steps of:

applying a source current to a reference cell to be evaluated; and

adjusting a gate voltage the reference cell to be evaluated until one of a stop and start of a predetermined level of current is sourced by the reference cell to be evaluated indicating a programmed state of the reference cell to be evaluated.

89.(New) The method according to claim 85, wherein:

said step of applying array cell evaluation voltages includes at least one step of,

applying at least one external voltage source to said selected array cell,

dividing at least one of an external voltage and an internal voltage source and applying the divided voltage to said selected array cell, and

retrieving a table register value indicating at least one voltage and applying the indicated voltages to said selected array cell; and

said step of applying reference cell evaluation voltages to a reference cell to be evaluated includes at least one step of,

applying at least one external voltage source to the reference cell to be evaluated,

dividing at least one of an external voltage and an internal voltage source and applying the divided voltage to the reference cell to be evaluated, and

retrieving a table register value indicating at least one voltage and applying the indicated voltages to the reference cell to be evaluated.

90.(New) A method of programming a reference cell in a device comprising the steps of:

programming a threshold voltage of said reference cell utilizing internal circuitry of the device;

verifying the programmed threshold of said reference cell; and

repeating said steps of programming and verifying until one of a max number of programming attempts has occurred and a predetermined threshold voltage is attained in said reference cell.

91.(New) A method of programming a reference cell in a device, comprising the step of:

programming a threshold voltage of said reference cell utilizing internal circuitry of the device, wherein said step of programming a threshold voltage comprises the steps of,

determining if said threshold voltage has at least attained a predetermined program level via a program verify operation;

if said threshold voltage has not attained said predetermined programmed level, then performing the step of,

programming the reference cell; and

repeating said steps of determining and programming until at least one of a max number of program attempts occurs and said predetermined program level is attained in said reference cell.

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92.(New) The method according to claim 91, further comprising the step of:

verifying the programmed threshold of said reference cell.

93.(New) A memory device, comprising:

at least one array cell configured to store data;

at least one reference cell configured to provide a reference for operations performed on said array cells;

means for performing said operations on said array cells utilizing said reference cells; and

means for programming said reference cells utilizing internal circuitry of said memory device.

94.(New) The memory device according to claim 93, wherein said memory device is a flash memory device.

95.(New) A memory device comprising:

at least one array cell configured to store data;

at least one reference cell configured to provide a reference for operations performed on said array cells;

means for performing said operations on said array cells utilizing said reference cells; and

means for programming said reference cells utilizing internal circuitry of said memory device, wherein said means for programming includes:

means for determining a threshold voltage (V_T) of a selected reference cell by comparing the selected reference cell to a selected array cell; and

means for programming the selected reference cell to a selected V_T based on the determined threshold voltage (V_T).

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96.(New) A memory device comprising:

at least one array cell configured to store data;

at least one reference cell configured to provide a reference for operations performed on said array cells;

means for performing said operations on said array cells utilizing said reference cells; and

means for programming said reference cells utilizing internal circuitry of said memory device, wherein said means for programming comprises:

means for producing high level voltages, internal to said device and controlled by said means for performing, for applying programming pulses to said reference cell arrays.